REMARKS/ARGUMENTS

Favorable reconsideration of this application, as presently amended and in light of the following discussion is respectfully requested.

After entry of the present amendment, Claims 1-13 are pending in the present application. The present amendment amends Claims 1 and 13 without introduction of new matter.

In the outstanding Office Action, Claims 1, 3, and 7 were rejected under 35 U.S.C. 102(e) as anticipated by U.S. Patent No. 6,294,834 to Yeh et al. (hereinafter "Yeh"); Claims 2, 4, and 8-13 were rejected under 35 U.S.C. 103(a) as unpatentable over Yeh in view of U.S. Patent No. 6,734,477 to Moise; Claim 5 was rejected under 35 U.S.C. 103(a) as unpatentable over Yeh in view of U.S. Patent No. 6,417,092 to Jain et al. (hereinafter "Jain"); and Claim 6 was rejected under 35 U.S.C. 103(a) as unpatentable over Yeh in view of Moise and Jain.

Turning now to the rejection of Claims 1, 3, and 7 under 35 U.S.C. 102(e) as anticipated by Yeh, that rejection is respectfully traversed.

Amended independent Claim 1 recites a second via "formed directly on" a first via. Similarly, amended independent Claim 13 recites a second via "connected directly to" a first via. The remaining claims depend from Claim 1.

Applicants' Figures 1, 8, and 9 illustrate non-limiting examples of the claimed first and second vias of Claims 1 and 13. As shown, a first via 51 formed on upper electrode 35 of a capacitor 33-35 is directly connected to a second via 60a.

The outstanding Office Action cites Yeh's Figure 1 as teaching each feature of Claim 1. However, for the reasons stated below, Yeh's Figure 1 does not disclose first and second vias connected directly to one another. Rather, Yeh's Figure 1 discloses first and second vias connected to one another through a metal wiring.

Applicants now refer to Attachment 1, which labels portions of Yeh's Figure 1, for purposes of explanation. More particularly, Attachment 1 labels a first via V1, second via V2, first wiring layer M1, and second wiring layer M2. The first via V1 is formed on upper electrode 38 and connected to the second via V2 through the first metal wiring M1. The second metal wiring M2 is formed on the second via V2. The above determinations as to which components are "vias" and which components are "metal wirings" are based upon Yeh's statement that "The via opening 44 is filled with a multilevel interconnects layer 52, which is electrically connected to the upper electrode 38 of the capacitor 32;"[1] and, moreover, Yeh's further statement that "[A]ll of multilevel interconnects layer 50, 52, 54 and 56 are formed in a dual damascene process after via openings 42, 44, 46 and 48 are formed."[2] The dual damascene process is known as a process for simultaneously forming a via connected to a metal wiring in an insulating interlayer. In view of the above, Applicants submit that a first via V1 and a first metal wiring M1 are formed by a first dual damascene process; and that a second via V2 and a second metal wiring M2 are formed by a second dual damascene process.

Applicants respectfully submit that the distinction between a "via" and "wiring layer" is recognized within the art. Further, Applicants respectfully submit that Yeh's first metal wiring M1 is clearly not a "via" as applied by Applicants' specification or as applied under the customary usage of that term by skilled artisans.[3] Rather, the first metal wiring M1 is a "wiring layer." Thus, as the metal wiring M1 is not a "via" as understood within the art, the metal wiring M1 does not teach the claimed second "via" directly connected to a first via (connected to an upper electrode of a capacitor).

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[1] Yeh, col. 3, lines 53-56.
[2] Yeh, col. 4, lines 7-8.
[3] See MPEP § 2111.01; stating, "It is the use of the words in the context of the written description and customarily by those skilled in the relevant art that accurately reflects both the 'ordinary' and the 'customary' meaning of the terms in the claims. *Ferguson Beauregard/Logic Controls v. Mega Systems*, 350 F.3d 1327, 1338, 69 USPQ2d 1001, 1009 (Fed. Cir. 2003)."

Accordingly, as Yeh does not teach or suggest the claimed first and second vias directly connected to one another, Applicants respectfully request that the rejection of Claims 1, 3, and 7 under 35 U.S.C. 102 as anticipated by Yeh be withdrawn.

Turning now to the rejections of Claims 2, 4-6, and 8-13 under 35 U.S.C. 103(a) as unpatentable over Yeh in view of Moise, summarized above, those rejections are respectfully traversed.

The outstanding Office Action cites Yeh's Figure 1 as disclosing the claimed inventions, with the exception of citing Moise as teaching the claimed cross areas of the first and second vias.[4] However, as the Action also cites Moise's Figure 1 as teaching the claimed features (by reference characters within parentheses), Applicants now address Moise's Figure 1 with respect to the first and second vias of Claims 1 and 13.

Moise's Figure 1 illustrates two metal layers M1, M2 on an upper electrode of a capacitor 50 or 52. Applicants refer to Attachment 2, which labels portions of Moise's Figure 1, for purposes of explanation. The Office Action appears to cite the first metal layer M1, which is formed on the upper electrode 66 of capacitor 50, as the claimed first via. The second metal layer M2, which is formed on the first metal layer M1 in the first metal level 18, does not teach the claimed second "via" because the second metal layer M2 does not connect upper and lower wirings. If the metal layer M2 were a "via" as understood within the art, then the metal layer M2 would be formed to connect overlying and underlying metal wirings. However, no overlying metal wiring is shown.

Accordingly, as neither Yeh nor Moise teaches or suggests the claimed first and second vias (directly connected to one another), Applicants respectfully request that the rejections of Claims 2, 4-6, and 8-13 under 35 U.S.C. 103(a) as unpatentable over Yeh in view of Moise, summarized above, be withdrawn.

[4] Office Action, 6/14/2005, page 4,

As noted above, Applicants submit that neither Yeh nor Moise teach first and second vias, as claimed and understood within the art. Applicants further submit that neither Yeh nor Moise teach the third and fourth vias of the dependent claims.

For instance, Claim 4 recites "wherein the predetermined wiring layer has a third via formed on the lower electrode [of the capacitor] and a wiring connected to the third via and buried in a surface of the predetermined wiring layer." The Office Action cites Moise's diffusion region 34 as teaching the claimed lower electrode. However, the diffusion region 34 is not part of the capacitor 62. Further, the diffusion region 34 is not connected to a wiring "buried in a surface of the predetermined wiring layer," as claimed.

Claims 9 and 10 recite "a third via formed on the lower electrode of the capacitor"; and "a fourth via formed connected to a top of the third via and formed to be thinner than the third via." The Office Action appears to cite the conductive components formed on the upper electrode 66 of Moise's capacitor 62 as teaching an underlying via (see layer 16) and a thinner overlying via (see layer 18), respectively. However, as noted above, the overlying conductive portion of layer 18 is not a "via" as understood by those skilled in the art. Thus, the overlying conductive portion of layer 18 cannot teach a thinner overlying via (such as the claimed fourth via)

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance, and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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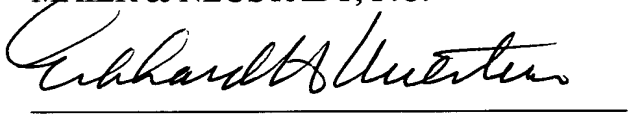
MAIER & NEUSTADT, P.C.



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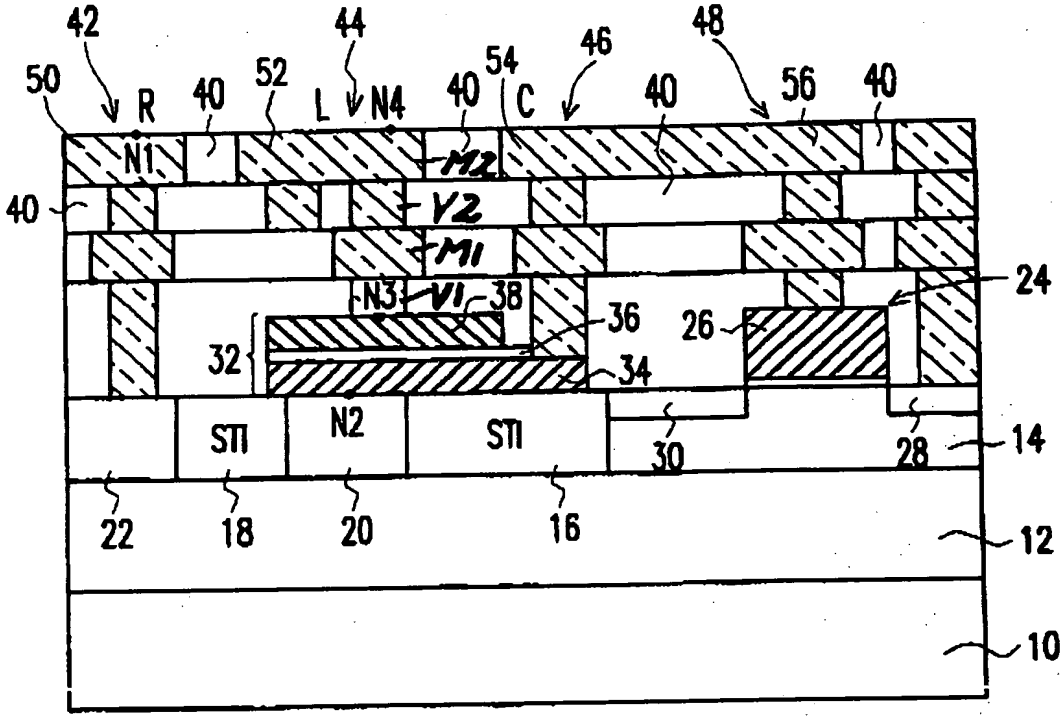

FIG. 1

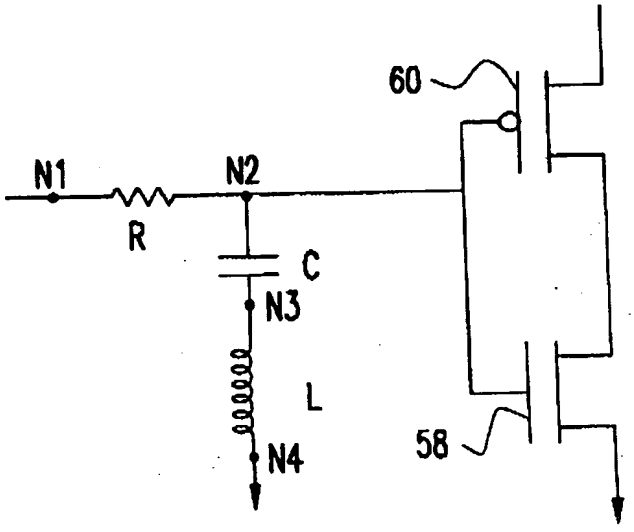

FIG. 2

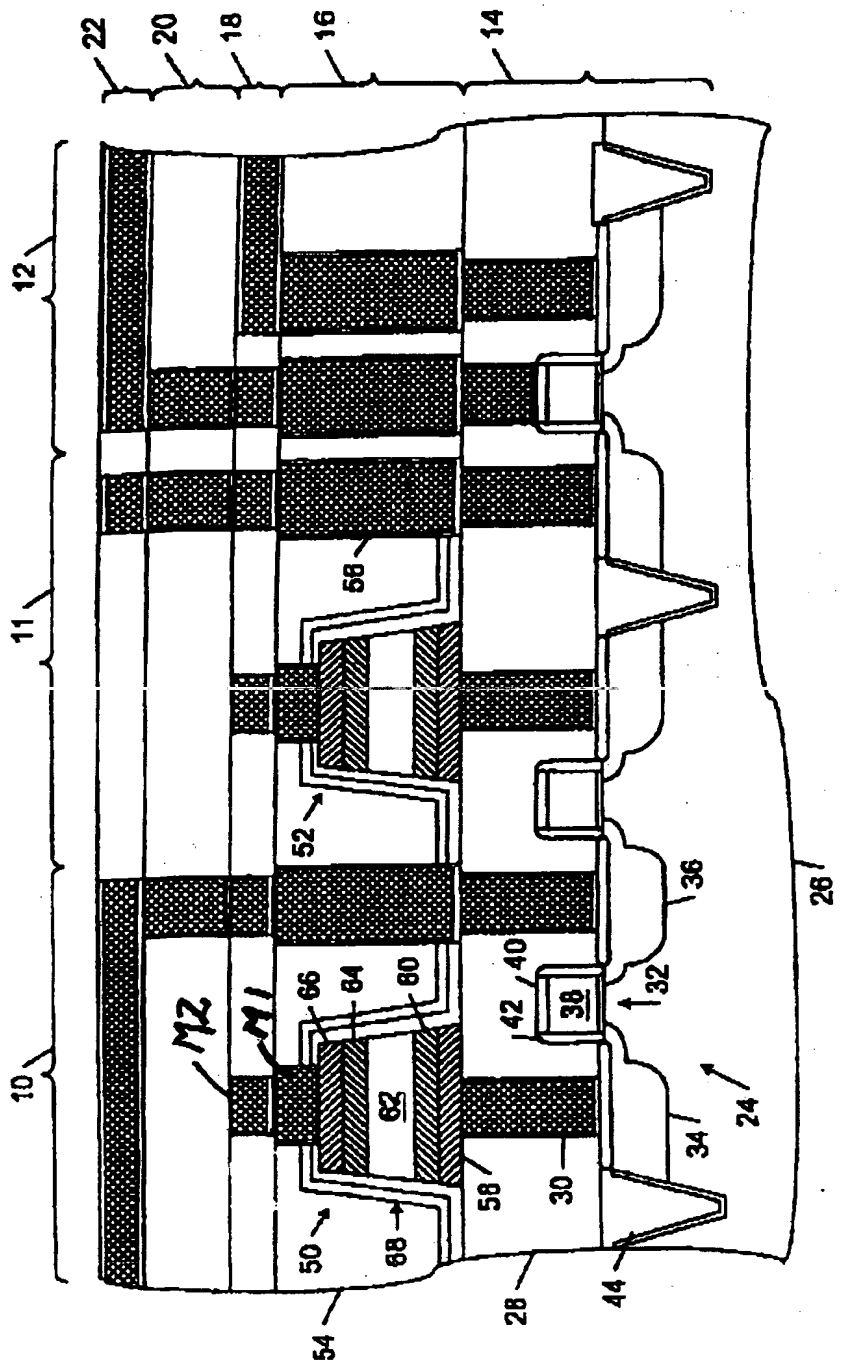
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FIG. 1